REMARKS/ARGUMENTS

Favorable reconsideration of this application in view of the above amendments and in light of the following discussion is respectfully requested.

Claims 23-31 are pending in this application. The present Amendment amends Claims 23, 25-29, and 31 without introducing any new matter.

In the outstanding Office Action, Claims 23, 24, and 29 were rejected under 35 U.S.C. § 102(e) as anticipated by Merchant et al. (U.S. Patent No. 6,118,181, hereinafter Merchant); Claims 25, 30, and 31 were rejected under 35 U.S.C. § 103(a) as unpatentable over Merchant in view of Goesele et al. (U.S. Patent No. 5,877,070, hereinafter Goesele) and Linn et al. (U.S. Patent No. 5,387,555, hereinafter Linn); and Claims 26-28 are rejected under 35 U.S.C. § 103(a) as unpatentable over Merchant in view of Doyle et al (U.S. Patent No. 6,423,614, hereinafter Doyle).

In order to clarify Applicant's invention, Claims 23, 29, and 31 are amended to recite "tungsten" instead of "metallic material," "SiC film" instead of "semiconductor film," and "carrying out a heat treatment at a temperature of or greater than 650° C" instead of "carrying out a heat treatment." Additionally, Claims 25-28 have been amended in a manner consistent with amended Claim 23. These features find non-limiting support in the disclosure as originally filed, for example at page 9, lines 7-31, with reference to Figures 2A-2D.

In light of the amendments to the independent claims, Applicants respectfully request reconsideration of the rejection of Claims 23, 24, and 29 under 35 U.S.C. § 102(e) as anticipated by Merchant, as next discussed.

Claim 23 as currently amended recites, *inter alia*:

> ...carrying out a heat treatment ***at a temperature of or greater than 650°C*** for combining the deposited layers to form one layer that provides an electrically conducting bonding between the two faces...

Merchant fails to describe every element of Claim 23 as currently amended. Merchant describes the bonding of two wafers, wherein a palladium (Pd) layer on the first wafer is engaged with a silicon (Si) layer from the second wafer, by annealing.[1] Merchant further explains that to bond the silicon layer (31) with the palladium layer, an annealing step below 450° C is used, to thereby create an electrically conducting bond between the layers.[2] In particular, Merchant states that the "bonding wafer may be of any suitable configuration as long as the bonding materials can be bonded at CMOS compatible temperatures,"[3] further noting that "'CMOS compatible' shall refer to a process or system that that prevents damage to CMOS components or other adverse effects from occurring due to exposure to temperatures above approximately 500 degrees Celcius."[4] However, Merchant fails to describe carrying out a heat treatment ***at a temperature of or greater than 650°C*** for combining the deposited layers to form one layer that provides an electrically conducting bonding between the two faces.

Further, as noted in the Office Action Merchant "is silent about the semiconductor element being SiC."[5] Claim 23 is presently amended to recite "SiC film" instead of "semiconductor film," thereby patentably defining over Merchant.

Further, Merchant does not describe "depositing at least one layer directly on the face of the second semiconductor element, each material chosen for each layer being either a semiconductor material or tungsten, wherein at least one layer deposited on the first and second semiconductor elements ***being of tungsten***" as defined in Claim 23. Instead, Merchant describes a silicon (Si) layer of the bonded wafer is preferably bonded to a palladium (Pd) layer of the handle wafer to form a bond between the two wafers.[6] The

---

[1] See Merchant in the Abstract.
[2] See Merchant, column 4, lines 8-19.
[3] See Merchant, column 4, lines 60-63.
[4] See Merchant, column 3, lines 24-28.
[5] See outstanding Office Action at page 6, section 14.
[6] See Merchant, column 3, lines 39-41.

palladium layer of Merchant is not at least one layer deposited on the first and second semiconductor elements ***being of tungsten*** as currently claimed.

Accordingly, as Merchant does not describe every feature recited in Claim 23 as currently amended, Claim 23 is not anticipated by Merchant and patentably defines over the cited art. Therefore, the rejection to Claim 23 and all claims dependent therefrom is traversed, and reconsideration of the rejection based on Merchant is requested.

Although different in scope, Claim 29 recites similar features. Accordingly, Accordingly, as Merchant does not describe every feature recited in Claim 29 as currently amended, Claim 29 is not anticipated by Merchant and patentably defines over the cited art. Therefore, the rejection to Claim 29 and all claims dependent therefrom is traversed, and reconsideration of the rejection based on Merchant is requested.

In light of the amendments to the independent claims, Applicants respectfully request reconsideration of the rejection to Claims 25 and 31 under 35 U.S.C. § 103(a) as unpatentable over Merchant in view of Goesele and Linn because there is insufficient evidence for a motivation to modify the Merchant system by incorporating Goesele's use of silicon carbide in the bonding process and Linn's use of tungsten, for the following reasons.

The outstanding Office Action states that it would have been obvious "to modify Merchant et al. reference by including the use of SiC as taught by Goesele et al. and the use of tungsten and the oxide layer as taught by Linn et al. because Merchant et al. suggested that other suitable elements may be used and would provide better stress compensation and less contamination."[7] The record, however, fails to provide the required **evidence** of a motivation for a person of ordinary skill in the art to perform such modification. While Linn may provide a reason for using tungsten or another material in combination with an oxide layer,[8]

---

[7] See outstanding Office Action at page 6, section 15.
[8] See Linn, for example, oxide layer 316 in Figure 2c and Figures 3a-3f; oxide layers 406 and 413 in Figures 4a-4d; and oxide layers 506 and 513 in Figures 5a to 5b).

Linn fails to suggest why a person of ordinary skill in the art at the time of the invention would be motivated to incorporate *only the tungsten without an oxide layer* in a system for wafer bonding such as the one disclosed in Merchant. In particular, Linn uses an oxide layer between the silicon film and the tungsten to protect the film from the migration of tungsten at high temperature.[9] Linn, however, does not suggest replacing the combination oxide layer + silicon film by a single SiC film suggested in Goesele for protecting the film from the diffusion of metallic species at high temperatures, while improving the electrical conductivity of the bonding.

Further, as discussed above, Merchant relates to a method where the temperature is maintained at low values, i.e. lower than 500°C. Particularly, it is indicated that these temperatures should be "CMOS-compatible". Therefore, upon review of Merchant, a person of ordinary skill in the art at the time of the invention the skilled in the art would have not have been motivated to employ a method using temperatures equal to or greater than 500°C. Specifically, Goesele teaches that "[f]or silicon carbide the wafer temperature during implantation is in the range of 500 degrees centigrade to 1,100 degrees centigrade."[10]

According, the rejection to Claims 25 and 31 under 35 U.S.C. § 103(a) as unpatentable over Merchant in view of Goesele and Linn are traversed because there is insufficient evidence for a motivation to modify the Merchant system by incorporating Goesele's use of silicon carbide in the bonding process and Linn's use of tungsten. Reconsideration of the rejection of Claims 25 and 31 as unpatentable over Merchant in view of Goesele and Linn is respectfully requested.

In light of the amendments to the independent claims, Applicants respectfully request reconsideration of the rejection to Claim 30 under 35 U.S.C. § 103(a) as unpatentable over Merchant in view of Goesele and Linn.

---

[9] See Linn at column 2, line 67-column 3, line 1.
[10] See Goesele, at column 11, line 67 to column 12, line 2.

Claim 30 depends from Claim 29 and thereby includes all of its features. Claim 29 recites, *inter alia*:

> ...combining the deposited layers to form one layer ***that provides an electrically conducting bonding*** between the two faces, no insulator layer being interposed between the two faces such that the second semiconductor element is not electrically insulated from the first semiconductor element...
>
> ...one of the layers is deposited with an excess thickness such that a part of this layer, in contact with another of the deposited layers, combines with the another deposited layer to form the stable mixture, the another layer deposited with an excess thickness, in contact with the semiconductor element on which it is deposited, reacting during the heat treatment with the semiconductor element ***to form a film with ohmic contact.***

The proposed combination fails to teach every element claimed in Claim 29. The Office Action asserts that the additional layer of chromium (Cr), titanium (Ti) or other suitable elements interposed between the metallic layer of (Pd) and the (Si) substrate described in Merchant at column 3, lines 30-66 with reference to Figure 1A discloses providing an excess thickness as recited in Claim 29. However, this additional layer is not the "layer deposited with an excess thickness, in contact with the semiconductor element on which it is deposited" as recited in Claim 29, since it does not react with the metallic material (Pd) or the semiconductor element (Si) to "form one layer ***that provides an electrically conducting bonding***," as currently claimed.

Further, Merchant does not teach this layer of (Cr) or of (Ti) "reacting during the heat treatment with the semiconductor element ***to form a film with ohmic contact***," as currently claimed.

Linn fails to cure the deficiencies found in Merchant. To the contrary, Linn teaches away from the features recited in Claim 29. Linn teaches low temperature silicon-on-insulator wafer bonding using a silicide bond formation reaction.[11] Linn further teaches that

[11] See Linn, the Abstract.

the resulting silicide layer acts as a barrier that protects the substrate from diffusion of contaminants, such as tungsten.[12] Specifically, Linn teaches an oxide layer between the conductor bonding and each one of the two substrates to be bonded when the temperature of the heat treatment is high.[13] Thus, by teaching an oxide layer between the conductor bonding and each of the two substrates to be bonded, Linn teaches away from forming a film with an ohmic contact, as currently claimed.

Regarding Goesele, these teachings were not cited with respect to the above-noted features regarding the film with an ohmic contact, and are not believed to overcome the above-noted deficiencies in Linn.

Accordingly, the combination of Merchant and Linn and Goesele fails to teach every element in Claim 29. Therefore, the rejection of Claim 30. which depends from Claim 29, is traversed, and reconsideration of the rejection based on Merchant in view of Linn and Goesele is requested.

In light of the amendments to the independent claims, Applicants respectfully request reconsideration of the rejection of Claims 26-28 under 35 U.S.C. § 103(a) as unpatentable over Merchant in view of Doyle.

Claims 26-28 depend from Claim 23 and therefore include all of the features recited in Claim 23. As discussed above, Merchant describes bonding a silicon layer with a palladium layer using an annealing step below 450° C to create an electrically conducting bond between the layers. Merchant fails to describe carrying out a heat treatment ***at a temperature of or greater than 650°C*** for combining the deposited layers to form one layer that provides an electrically conducting bonding between the two faces as currently claimed in Claim 23. Doyle fails to cure this deficiency. As can be seen, for example, at column 3, lines 59-66, Doyle describes bonding substrate layers at temperatures of approximately 400°

[12] See Linn, at column 5, lines 1-29.
[13] See Linn, at column 6, line 41 to column 7, line 49; and column 8, lines 31-32.

C. Bonding substrate layers at approximately 400° C is not carrying out a heat treatment at a temperature of or greater than 650° C for combining the deposited layers to form one layer that provides an electrically conducting bonding between the two faces as currently claimed. Therefore, even if the combination of Merchant and Doyle is assumed to be proper, the combination fails to teach every element of the claimed invention.

Accordingly, the combination of Merchant and Doyle fails to teach every element in Claim 23. Therefore, the rejection of Claims 26-28 depending from Claim 23 is traversed, and reconsideration of the rejection based on Merchant in view of Doyle is requested.

Consequently, in view of the present Amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal Allowance. A Notice of Allowance for Claims 23-31 is earnestly solicited.

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, the Examiner is encouraged to contact the Applicant's undersigned representative at the below listed telephone number.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

Gregory J. Maier
Attorney of Record
Registration No. 25,599

Surinder Sachar
Registration No. 34,423

GJM:SNS:CB\la
I:\ATTY\CAB\22's\220040US\220040US-REPLY-TO-OA-OF-06052006.DOC